

DATA SHEET

PDTC143Z series

NPN resistor-equipped transistors;

$R1 = 4.7 \text{ k}\Omega$, $R2 = 47 \text{ k}\Omega$

Product specification
Supersedes data of 2004 Apr 06

2004 Aug 16

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FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	4.7	–	k Ω
R2	bias resistor	47	–	k Ω

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC143ZE	SOT416	SC-75	38	PDTA143ZE
PDTC143ZEF	SOT490	SC-89	53	PDTA143ZEF
PDTC143ZK	SOT346	SC-59	18	PDTA143ZK
PDTC143ZM	SOT883	SC-101	E3	PDTA143ZM
PDTC143ZS	SOT54 (TO-92)	SC-43	TC143Z	PDTA143ZS
PDTC143ZT	SOT23	–	*18 ⁽¹⁾	PDTA143ZT
PDTC143ZU	SOT323	SC-70	*54 ⁽¹⁾	PDTA143ZU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC143ZS	MAM364	1 2 3	base collector emitter
PDTC143ZE PDTC143ZEF PDTC143ZK PDTC143ZT PDTC143ZU	Top view MDB269	1 2 3	base emitter collector
PDTC143ZM	bottom view MHC506	1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC143ZE	–	plastic surface mounted package; 3 leads	SOT416
PDTC143ZEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC143ZK	–	plastic surface mounted package; 3 leads	SOT346
PDTC143ZM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC143ZS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC143ZT	–	plastic surface mounted package; 3 leads	SOT23
PDTC143ZU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage				
	positive		–	+30	V
	negative		–	–5	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT883	notes 2 and 3	–	250	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT883	notes 2 and 3	500	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

CHARACTERISTICS

$T_{amb} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}$; $I_E = 0 \text{ A}$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$	–	–	1	μA
		$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$; $I_C = 0 \text{ A}$	–	–	170	μA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}$; $I_C = 10 \text{ mA}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}$; $I_B = 0.25 \text{ mA}$	–	–	100	mV
$V_{i(off)}$	input-off voltage	$I_C = 100 \text{ }\mu\text{A}$; $V_{CE} = 5 \text{ V}$	–	0.6	0.5	V
$V_{i(on)}$	input-on voltage	$I_C = 5 \text{ mA}$; $V_{CE} = 0.3 \text{ V}$	1.3	0.9	–	V
R_1	input resistor		3.3	4.7	6.1	$\text{k}\Omega$
$\frac{R_2}{R_1}$	resistor ratio		8	10	12	
C_c	collector capacitance	$I_E = I_e = 0 \text{ A}$; $V_{CB} = 10 \text{ V}$; $f = 1 \text{ MHz}$	–	–	2.5	pF

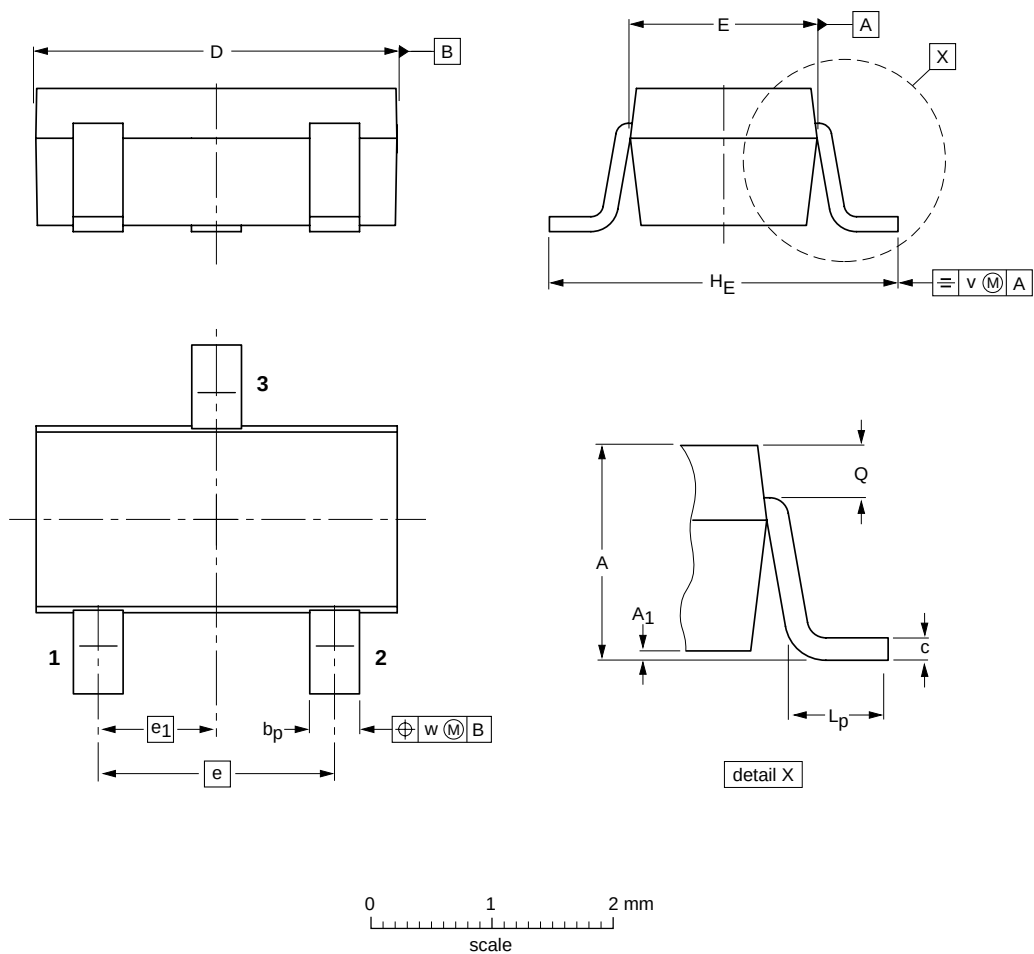
NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 47 kΩ

PDTC143Z series

PACKAGE OUTLINES

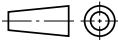
Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

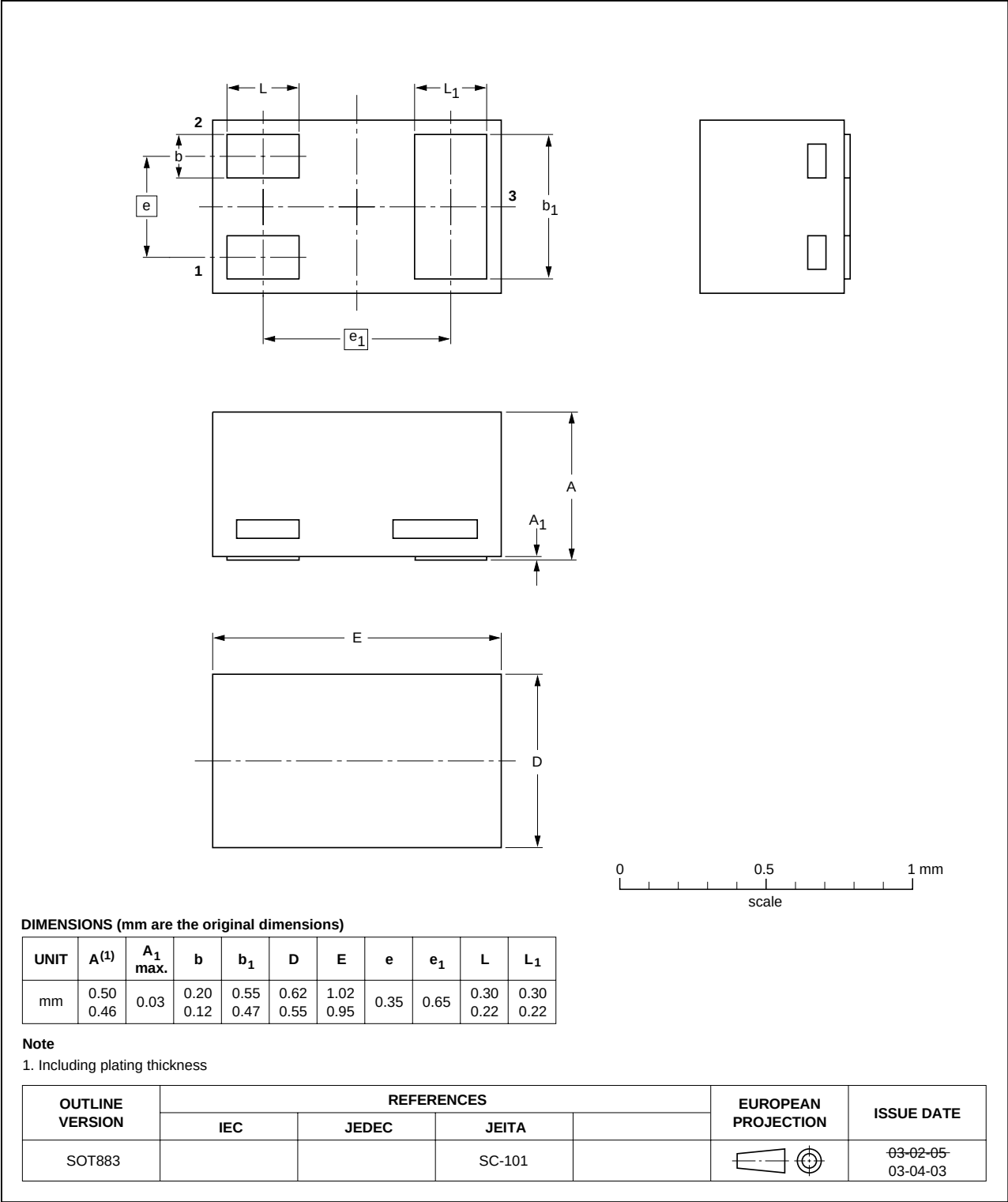
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

NPN resistor-equipped transistors;
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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

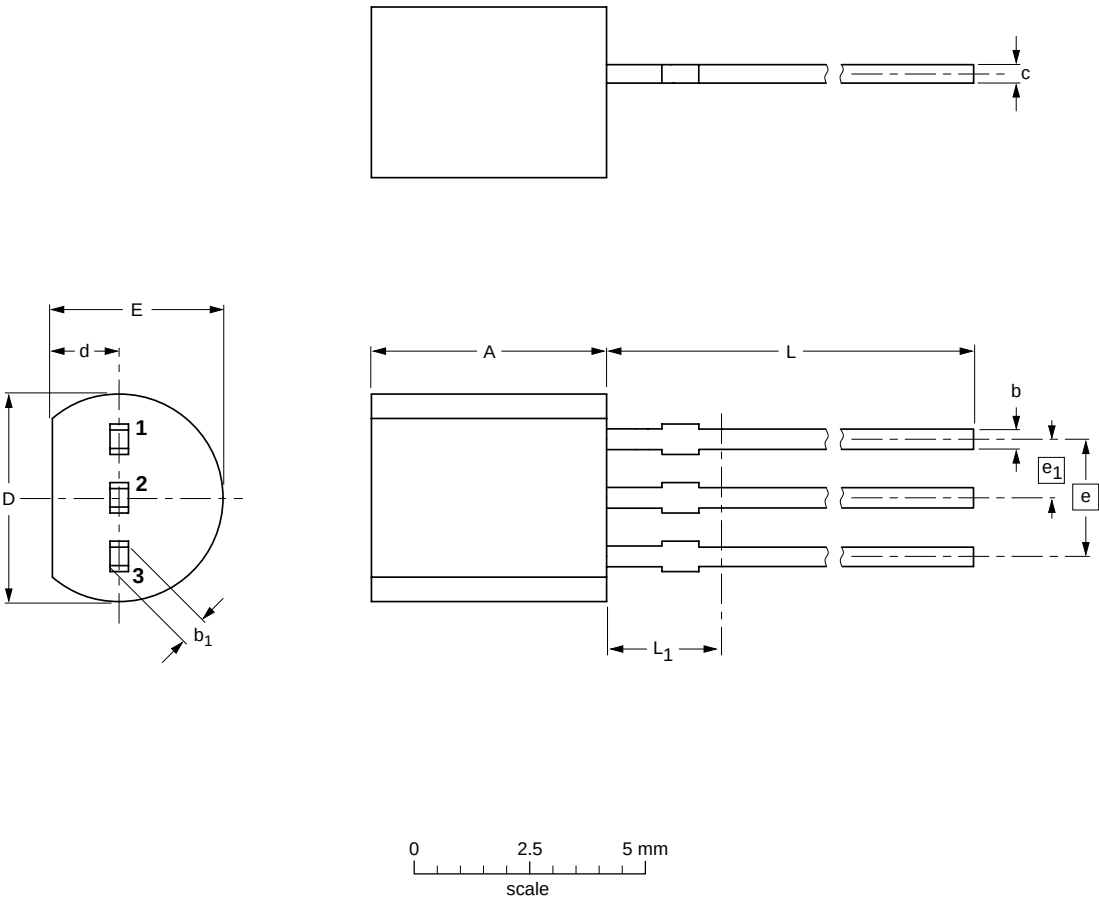


NPN resistor-equipped transistors;
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PDTC143Z series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note
1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

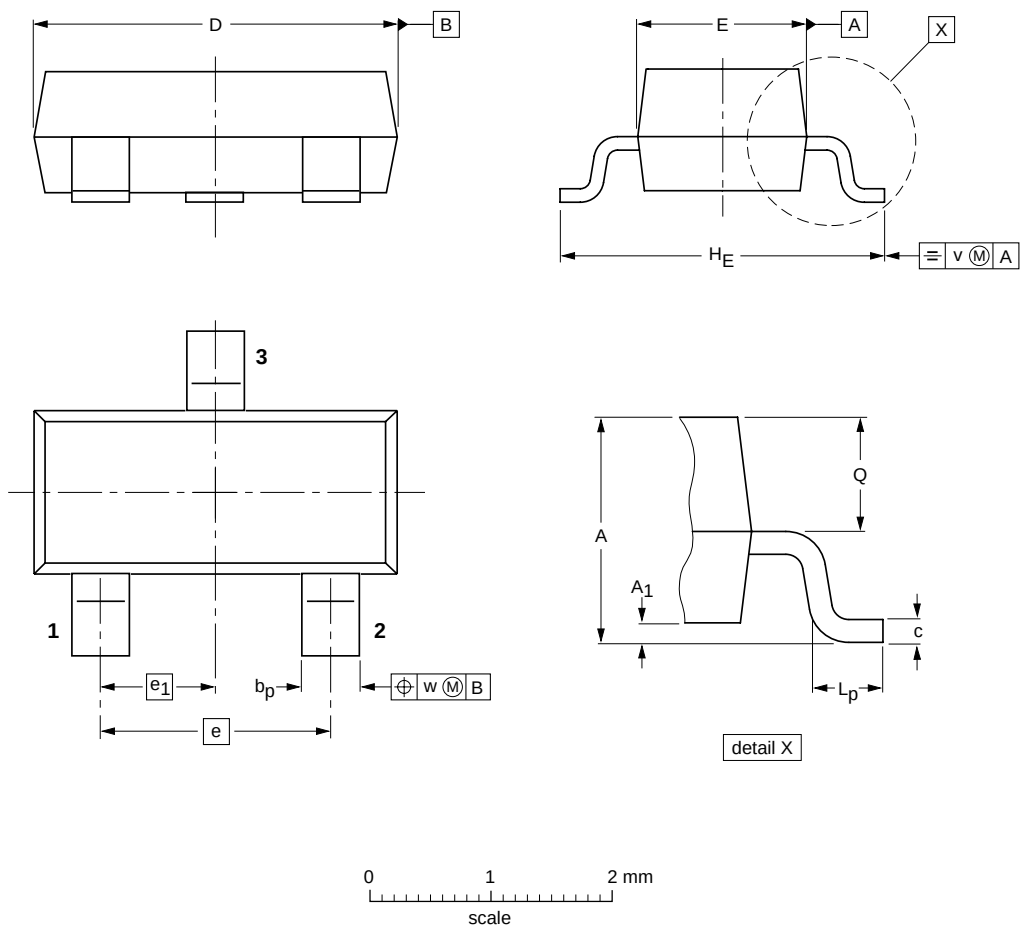
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			-97-02-28 04-06-28

NPN resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

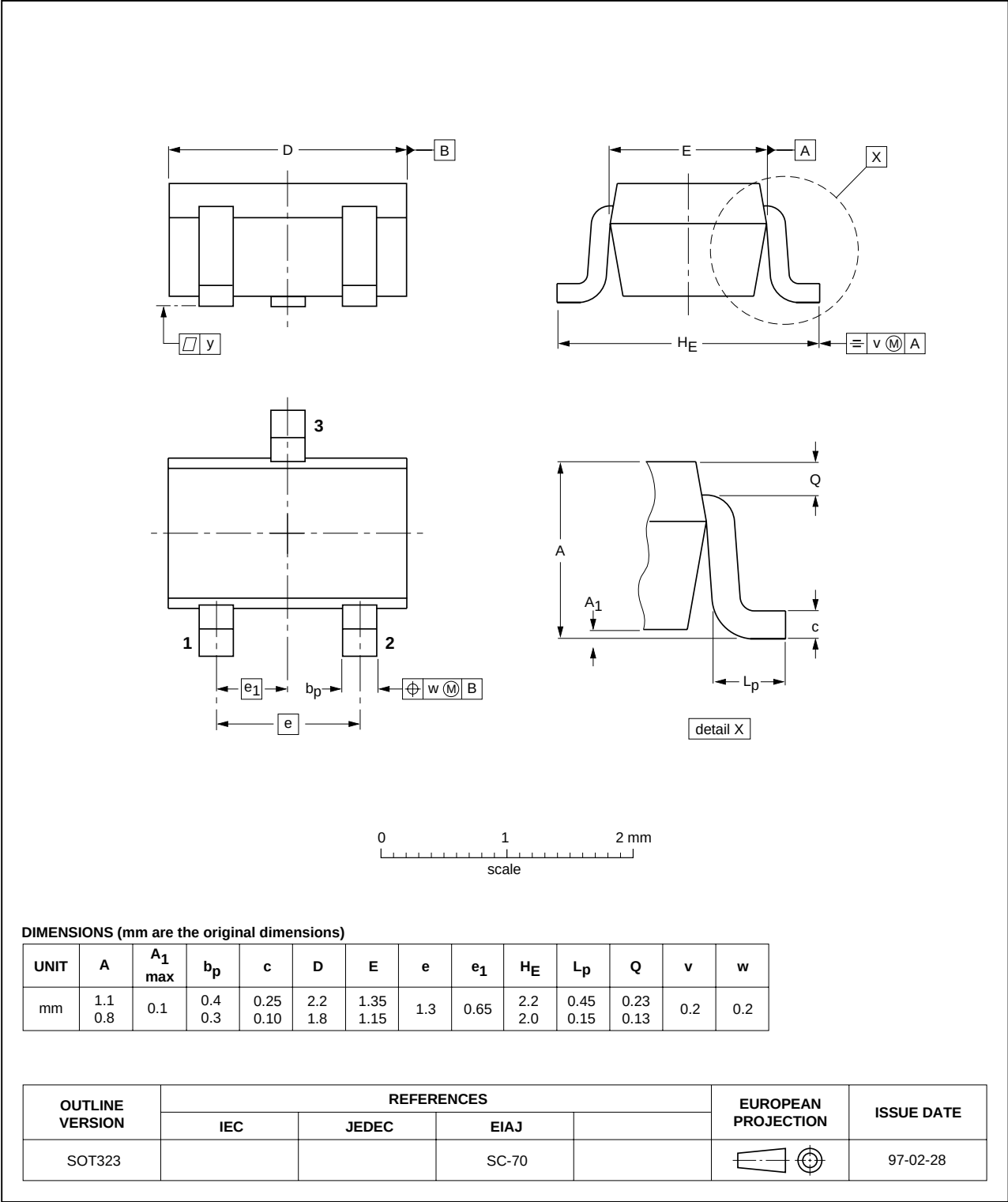
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28 99-09-13

NPN resistor-equipped transistors;
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PDTC143Z series

Plastic surface mounted package; 3 leads

SOT323

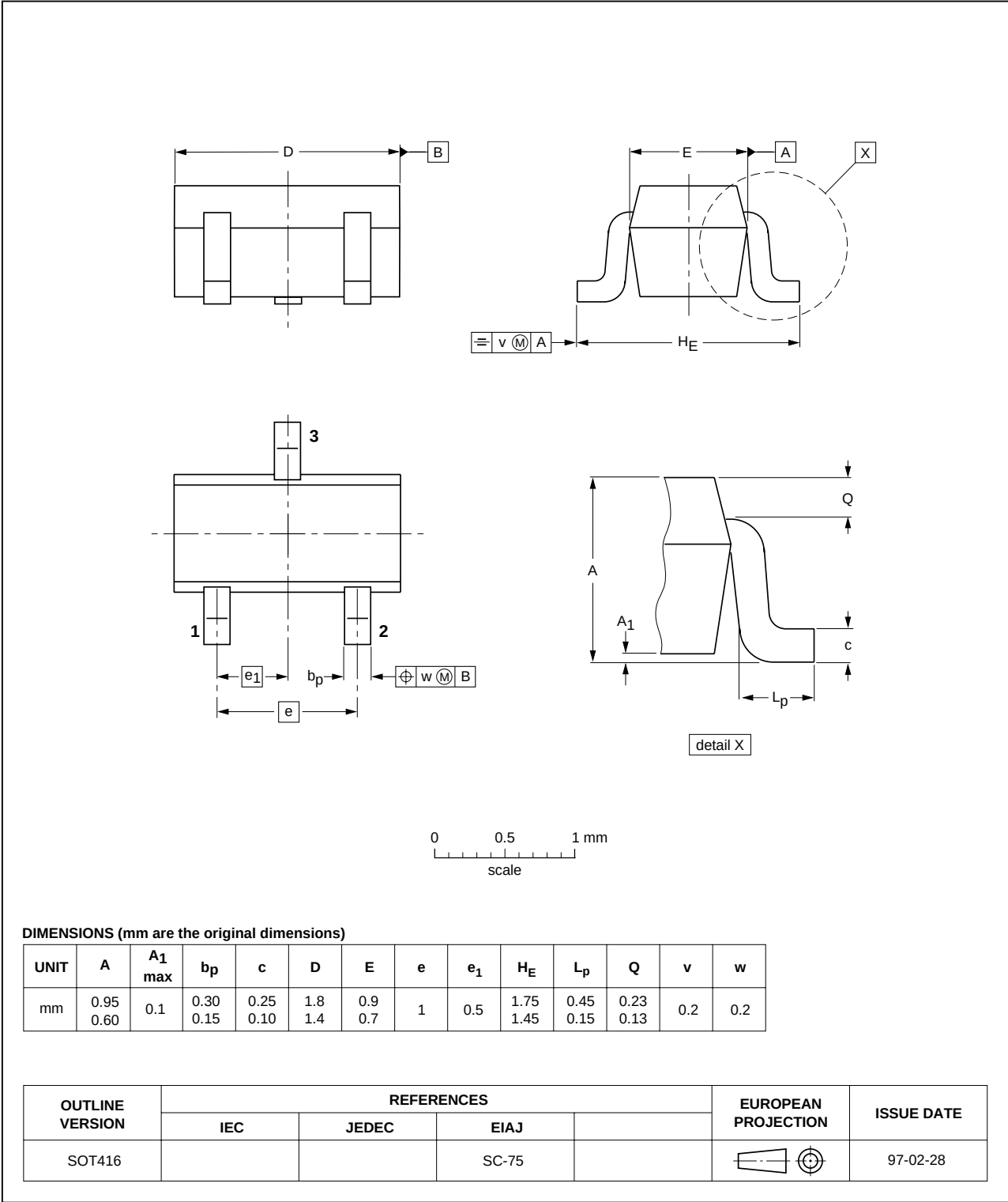


NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 47 kΩ

PDTC143Z series

Plastic surface mounted package; 3 leads

SOT416

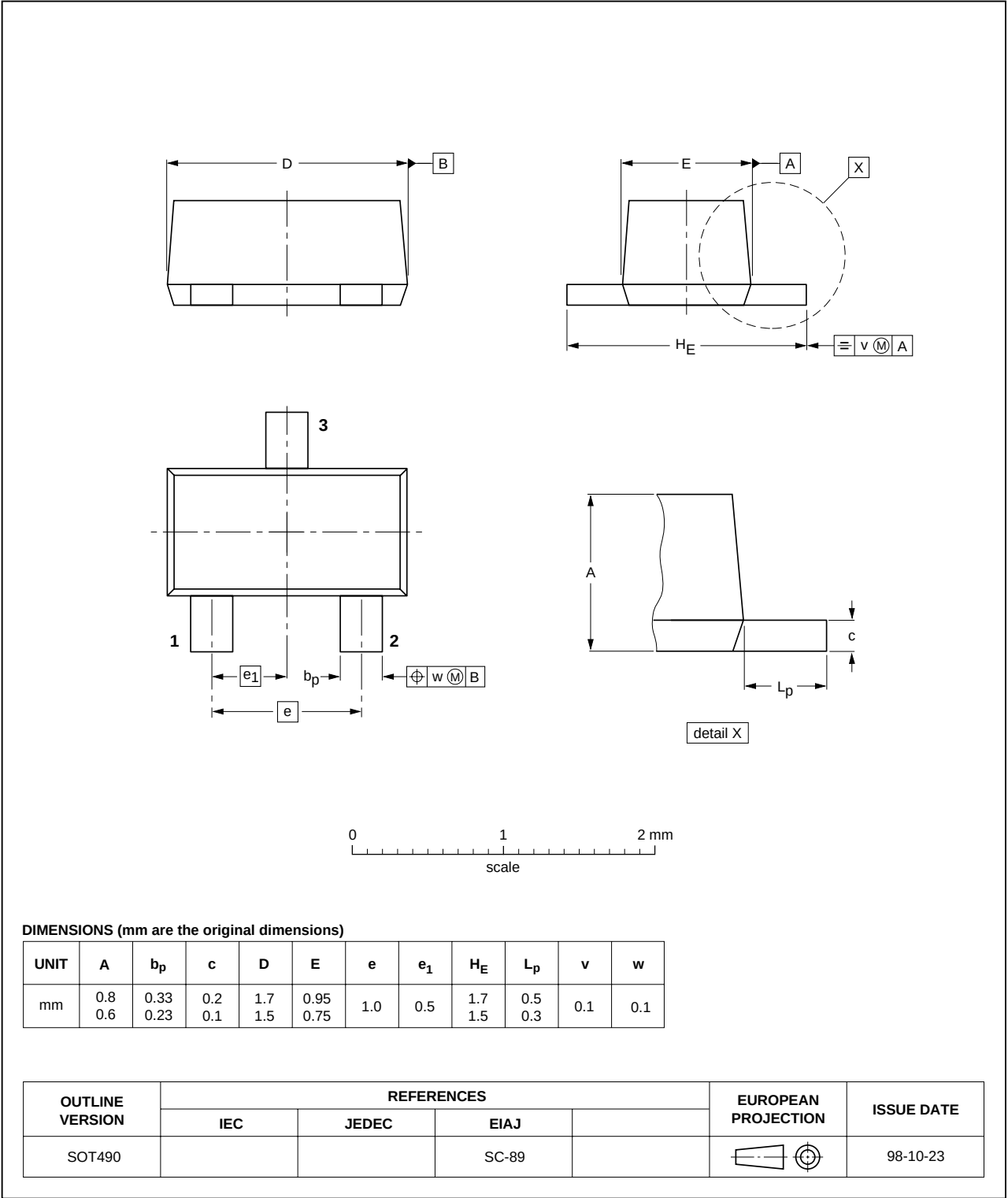


NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 47 kΩ

PDTC143Z series

Plastic surface mounted package; 3 leads

SOT490



NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 47 kΩ

PDTC143Z series

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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Notes

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

R75/07/pp14

Date of release: 2004 Aug 16

Document order number: 9397 750 13677

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